Patent Application
Docket No. 02-C-086

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Date of Deposit: June 24, 2003
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Name: Carolyn Bova

Signature: Carolyn Bova

STARTUP CIRCUIT AND METHOD FOR OSCILLATOR CIRCUITRY

BACKGROUND OF THE INVENTION

Technical Field of the Invention

The present invention relates to starting an oscillator, and particularly to a circuit and method for starting an oscillator shortly after power-up.

Description of the Related Art

Crystal oscillators have been used in the electronics industry for decades for providing a clock or other signal having a fixed, predetermined frequency. Some existing crystal oscillator circuits receive an enable signal to enable the crystal oscillator circuit to oscillate at the desired frequency at a time during system operation selected

and controlled by the system in which the oscillator circuit is located. A shortcoming, however, with this type of system-controlled operation is that some systems may not be capable of controlling the time at which an oscillator circuit is to be enabled to oscillate. What is needed, then, is an oscillator circuit that quickly and easily commences oscillating substantially without additional system control or other overhead.

SUMMARY OF THE INVENTION

Embodiments of the present invention overcome the above-described shortcomings in existing crystal oscillator circuits and satisfy a significant need for a crystal oscillator circuit that will quickly and easily commence oscillating. In an exemplary embodiment of the present invention, the oscillator circuit is initially disabled from oscillating and enabled a period of time following the oscillator circuit being initially powered up, such as a predetermined period of time following the completion of a power-up sequence and/or a power-on-reset signal transitioning from a reset state to a non-reset state. The

oscillator circuit may include a counter to define the predetermined period of time. By delaying the commencement of the oscillations by the oscillator circuit until after power applied thereto has stabilized, the oscillator circuit is better ensured to oscillate relatively soon after the oscillator circuit is powered up.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete understanding of the system and method of the present invention may be obtained by reference to the following Detailed Description when taken in conjunction with the accompanying Drawings wherein:

Figure 1 is a block diagram of oscillator circuitry according to an exemplary embodiment of the present invention; and

Figure 2 is a schematic drawing showing an implementation of a portion of the oscillator circuitry of Figure 1 according to an exemplary embodiment of the present invention;

Figure 3 is a schematic drawing showing another implementation of a portion of the oscillator circuitry of

Figure 1 according to an exemplary embodiment of the present invention;

Figure 4 is a flow chart illustrating an operation of the oscillator circuit of Figure 1 according to an exemplary embodiment of the present invention; and

Figure 5 is a diagram of a system containing the oscillator circuitry of Figure 1.

DETAILED DESCRIPTION OF THE EXEMPLARY EMBODIMENTS

The present invention will now be described more fully hereinafter with reference to the accompanying drawings in which exemplary embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as being limited to the embodiments set forth herein. Rather, the embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art.

Referring to Figure 1, there is shown oscillator circuitry 1 according to an exemplary embodiment of the present invention. In general terms, oscillator circuitry

1 generates an output signal OSC-OUT that oscillates between at least two logic levels approximately at a predetermined frequency, starting a predetermined period of time following completion of a system power-up sequence.

Oscillator circuitry 1 may include a crystal oscillator circuit 5 for generating output signal OSC-OUT. Oscillator circuit 5 may include crystal 2, a logic inverter 3 coupled between the terminals of crystal 2, and a pair of capacitors 4 (see Figure 2). Each capacitor 4 may include a first plate terminal coupled to a distinct terminal of crystal 2 and a second terminal coupled to a reference voltage, such as ground. The operation of crystal 2, logic inverter 3 and capacitors 4 as shown in Figure 1 is known in the art and will not be described further for reasons of simplicity.

It is understood that crystal oscillator circuit 5 may have other implementations to cause output signal OSC-OUT to oscillate. It is further understood that the oscillator circuit 5 may be implemented without a crystal and nevertheless generate an output signal OSC-OUT that oscillates between at least two voltage levels and/or between at least two states.

Oscillator circuitry 1 may further include an enable circuit 6 for enabling the above-described crystal oscillator circuit 5 to oscillate. Enable circuit 6 may generate a signal, ENABLE, that is provided to the crystal oscillator circuit 5 to enable the crystal oscillator circuit 5 to oscillate. When in an active state, signal ENABLE enables the crystal oscillator circuit 5 to oscillate and thereby cause output signal OSC-OUT to oscillate between at least two logic levels. When in an inactive state, signal ENABLE disables the crystal oscillator circuit from oscillating, thereby causing output signal OSC-OUT to be fixed at one of the logic levels. In the exemplary embodiment of oscillator circuitry 1 shown in Figure 1, the active state for signal ENABLE is a logic low (logic zero), and the inactive state is a logic high (logic one). However, it is understood that the active state of signal ENABLE may be a logic high (logic one) and the inactive state of signal ENABLE may be a logic low.

Enable circuit 6 may include a start input for receiving a start-up signal START. Enable circuit 6 is adapted to delay the enabling of the crystal oscillator circuit 5 to

oscillate for a predetermined period of time following the start-up signal START transitioning from an inactive state to an active state. In order to provide for the delay of a predetermined period of time, enable circuit 6 may include a counter 7 having an output signal that generates the signal ENABLE and a control input coupled to signal START, and a ring oscillator 8 which generates a clock signal that is applied to the clock input of counter 7. The signal START, when placed in the inactive state, places counter 7 in a predetermined state. In the exemplary embodiment shown in Figure 1, the control input of counter 7 is a reset input for selectively resetting counter 7. It is understood, though, that the control input of counter 7 may be used to place counter 7 in other states, such as a set state in which each latch/flip-flop element forming counter 7 is placed in a logic high state, or a state in which the latch/flip-flop elements of counter 7 are not all placed in the same state.

When powered and operational, ring oscillator 8 generates an oscillating signal at a predetermined frequency. Ring oscillator 8 may include an odd number of logic inverters connected together to form a loop. Following

counter 7 starting in the reset state, application of the oscillating signal to counter 7 results in the output thereof toggling from one logic state to another after a predetermined number of cycles of the oscillating signal has elapsed. In this way, enable circuit 6 enables crystal oscillator circuit 5 after a predetermined period of time following counter 7 being activated by signal START.

It is understood that each of counter 7 and ring oscillator 8 may have any of a number of different circuit implementations, as is known in the art.

Oscillator circuitry 1 is adapted to be used in an electronics system requiring an oscillating signal. In the exemplary embodiment of the present invention, crystal oscillator circuit 5 is enabled to oscillate shortly after completion of a system power-up sequence. In this regard, oscillator circuitry 1 is adapted to receive at its START input a power-on-reset signal POR. Power-on-reset signal POR may be generated to provide a transition from a reset logic state (which resets or initializes circuitry in the system) to a non-reset state upon completion of the system power-up sequence and/or following the system being powered. In this

way, counter 7 of enable circuit 6 will be in a fixed state, such as the reset state, initially upon the system being powered up, and, subsequent to the power-up sequence, will begin counting.

Figure 2 shows a circuit implementation of oscillator circuitry 1 according to an exemplary embodiment of the present invention. In particular, the circuit implementation of Figure 2 shows how crystal oscillator circuit 5 is enabled by signal ENABLE. Crystal oscillator circuit 5 may include a transistor 9. Transistor 9 may be coupled across one of the capacitors 4. In this way, signal ENABLE turns on transistor 9 and thereby disables crystal oscillator circuit 5 from oscillating when signal ENABLE is in the inactive (logic high) state. Signal ENABLE turns off transistor 9 and thereby enables crystal oscillator circuit 5 to oscillate when signal ENABLE is in the active (logic low) state.

Figure 3 illustrates oscillator circuitry 30 according to another exemplary embodiment of the present invention. In this embodiment, crystal oscillator circuit 5 is provided current from a current source 31. Current source 31 may be

enabled to provide current to crystal oscillator circuit 5 by signal ENABLE using enable control circuitry 32.

Current source 31 may be implemented as a current mirror having a first current leg 33 including a p-channel transistor 34 and an n-channel transistor 35 coupled thereto, a second current leg 36 having a p-channel transistor 37 and an n-channel 38, and a third current leg having a p-channel transistor 39 that provides current to oscillator circuit 5 when activated. The control terminals of p-channel transistors 34, 37 and 39 are connected together, and the control terminals of n-channel transistors 35 and 38 are connected together. It is understood that the transistors in second current leg 36 and the third current leg may be sized proportionally to the transistors in first current leg 33 so as to provide the desired current levels in the second and third current legs, respectively. Nodes PBIAS and NBIAS in current source 31 may refer to the nodes at the control terminals of the p-channel transistors and the n-channel transistors of current source 31, respectively.

It is understood that current source 31 may be implemented in other ways so that signal ENABLE controls

whether or not current is provided to crystal oscillator circuit 5 and thus whether or not crystal oscillator circuit 5 oscillates.

Enable control circuitry 32 is adapted to receive the signal ENABLE and control current source 31 to selectively provide current to oscillator circuitry 5. Enable control circuitry 32 may include a logic inverter 40 which receives signal ENABLE and generates a logically inverted version thereof. A pulse generator circuit 41 may receive the output of logic inverter 40 and generate a pulse at an output upon the output of logic inverter 40 transitioning between logic states. For instance, pulse generator 41 may generate at its output a positive going pulse when the input of pulse generator 41 transitions from a logic high state to a logic low state. The output of pulse generator 41 may be coupled to a control transistor 42, which may have a first conduction terminal coupled to node PBIAS in current source 31 and a second conduction terminal coupled to node NBIAS therein. When activated, control transistor 42 may serve to short nodes PBIAS and NBIAS together.

A second control transistor 43 in enable control circuitry 32 may be coupled between the high reference voltage Vcc and node PBIAS and have a control terminal coupled to the output of logic inverter 40. A third control transistor 44 may be coupled between the low reference voltage Vss and node NBIAS and have a control terminal coupled to signal ENABLE. Second control transistor 43 serves to couple node PBIAS to the high reference voltage Vcc when activated, and third control transistor 44 serves to couple node NBIAS to the low reference voltage Vss when activated. By activating second control transistor 43 and third control transistor 44, the transistors in current source 31 are deactivated, thereby deactivating current source 31 and preventing current from being sourced to oscillator circuitry 5.

The operation of the oscillator circuitry of the present invention will be described with reference to Figure 4. Initially, a power-up sequence begins and/or power is provided to the system in which the oscillator circuitry is located. The supply voltage may, for example, ramp upwardly from the ground voltage. During this time, power-on-reset

signal POR is placed in the reset state, which in the exemplary embodiments is a logic low value. Signal POR being in the reset state causes counter 7 to be reset and to remain in the reset state regardless of the signal appearing at the clock input of counter 7.

Counter 7 being in the reset state causes signal ENABLE to be in an inactive state (logic high, in this case). With respect to the oscillator circuitry of Figure 2, signal ENABLE being in the logic high state activates transistor 9 and prevents crystal oscillator circuit 5 from oscillating. With respect to the oscillator circuitry of Figure 3, signal ENABLE being in the logic high state activates second control transistor 43 and third control transistor 44, which thereby causes nodes PBIAS and NBIAS to be in logic high and logic low states, respectively, so that current source 31 fails to conduct current. Without current sourced by current source 31, oscillator circuitry 5 is prevented from oscillating.

At or around the end of the power-up sequence, system circuitry and/or power-on-reset circuitry causes signal POR to transition to the non-reset logic state. This results in counter 7 no longer being held in the reset state and thereby

being enabled to count clock signals appearing at its clock input. Around the time of the power-up sequence, ring oscillator 8 commences oscillating, which causes its output signal to oscillate. Being enabled, counter 7 counts a predetermined number of clock cycles appearing on its clock input (i.e., the output of ring oscillator 8). When the predetermined number of clock cycles appearing on the clock input of counter 7 has elapsed, signal ENABLE is driven by counter 7 from the inactive state to the active state (logic low state). With regard to the oscillator circuitry of Figure 2, signal ENABLE being in the active state turns off transistor 9 and enables crystal oscillator circuit 5 to oscillate. With regard to the oscillator circuitry of Figure 3, signal ENABLE being in the active (logic low) state turns off control transistors 43 and 44 and causes pulse generator 41 to generate a positive-going pulse at its output. This pulse temporarily activates control transistor 42 so as to short together nodes PBIAS and NBIAS at a voltage level that is sufficient to turn on the transistors in current source 31. After completion of the pulse, the control transistors 42-44 in enable control circuitry 32 are deactivated so that

current is able to flow in each current leg of current source 31, which thereby results in current being provided to oscillator circuitry 5 for oscillation.

By delaying the time when crystal oscillator circuit 5 oscillates until system power has stabilized, crystal oscillator circuit 5 is better ensured to begin oscillating properly and quickly.

Figure 5 illustrates a system 50 in which the oscillator circuitry of the present invention may be disposed. System 50 may include the oscillator circuitry according to the embodiments of the present invention, and circuitry 52 that receives the output signal OSC-OUT for use as a clock signal, some other type of synchronization signal, etc. System 50 may be any type of system, such as a telecommunications system, an automotive-related system and a computer system.

The invention being thus described, it will be obvious that the same may be varied in many ways. Such variations are not to be regarded as a departure from the spirit and scope of the invention, and all such modifications as would be obvious to one skilled in the art are intended to be included within the scope of the following claims.